

Silicon PNP Power Transistors

2SA808

DESCRIPTION

- With TO-3 package
- Wide area of safe operation
- Complement to type 2SC1619

APPLICATIONS

- For power amplifier and general purpose applications

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

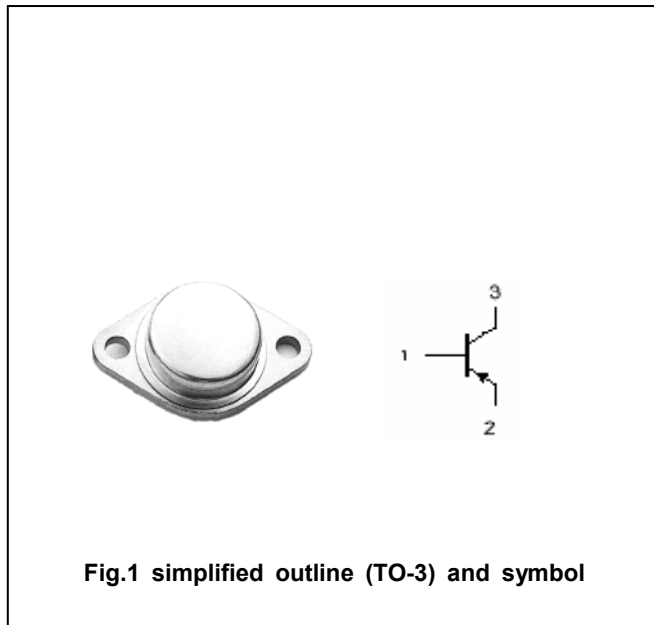


Fig.1 simplified outline (TO-3) and symbol

Absolute maximum ratings($T_a = \square$)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	-80	V
V_{CEO}	Collector-emitter voltage	Open base	-80	V
V_{EBO}	Emitter-base voltage	Open collector	-6	V
I_C	Collector current		-6	A
I_B	Base current		-3	A
P_C	Collector power dissipation	$T_C = 25 \square$	50	W
T_j	Junction temperature		150	\square
T_{stg}	Storage temperature		-65~150	\square

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CHARACTERISTICS

T_j=25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =-50mA I _B =0	-80			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =-3A; I _B =-0.3A			-1.5	V
I _{CBO}	Collector cut-off current	V _{CB} =-80V; I _E =0			-1.0	mA
I _{EBO}	Emitter cut-off current	V _{EB} =-6V; I _C =0			-1.0	mA
h _{FE}	DC current gain	I _C =-3A ; V _{CE} =-4V	20			
f _T	Transition frequency	I _C =-0.5A ; V _{CE} =-12V		10		MHz

Switching times

t _r	Rise time	V _{CC} =-10V; I _C =-3A; R _L =3Ω I _{B1} =-0.3A; I _{B2} =50mA		1.2		μs
t _{stg}	Storage time			1.8		μs
t _f	Fall time			0.3		μs

PACKAGE OUTLINE

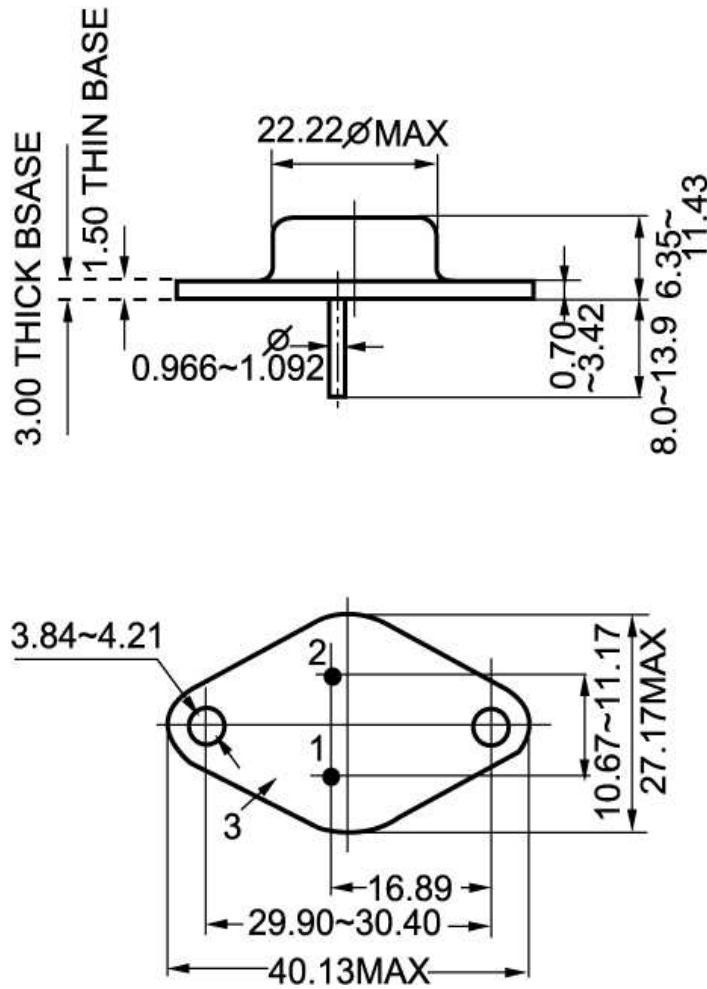


Fig.2 outline dimensions (unindicated tolerance:±0.1mm)